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# A SPUR-FREE FRACTIONAL-N $\Sigma\Delta$ PLL FOR GSM APPLICATIONS: LINEAR MODEL AND SIMULATIONS

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## ABSTRACT

A new PLL topology and a new simplified linear model are presented. The new  $\Sigma\Delta$  fractional-N synthesizer presents no reference spurs and lowers the overall phase noise, thanks to the presence of a Sample/Hold block. With a new simulation methodology it is possible to perform very accurate simulations, whose results match closely those obtained with the linear PLL model developed.

## 1. INTRODUCTION

$\Sigma\Delta$  modulation in fractional-N synthesizer is a technique that has been successfully demonstrated for high resolution and high speed frequency synthesizers [1, 2]. The use of high-order multi-bit  $\Sigma\Delta$  modulators introduces new issues which need to be carefully taken into account, such as down-folding of high frequency quantization noise, derivation of a linear model for noise analysis [4] and efficient techniques for fast and accurate simulations. The paper is organized as follows: in section 2 we present a new PLL topology which prevents high frequency noise down-folding and cancels reference spurs in the output spectrum. In section 3 the derivation of a linear model is presented. The resulting linear model is similar to [4], but the derivation is more straightforward. Section 4 presents a simple event-driven simulation approach, which compared to previous approaches [5, 3], offers greatly increased accuracy and simulation speed. Finally in section 5 we compare the theory developed with the results from simulations.

## 2. SPURS FREE PLL TOPOLOGY

The proposed synthesizer is shown in Fig. 1. The structure is similar to ordinary  $\Sigma\Delta$  fractional-N synthesizers except for the presence of a Sample-Hold (S/H) block between the Charge Pump (CP) and the Loop Filter (LF). The S/H serves two purposes: it prevents noise down-folding due to non-uniform sampling, and it cancels reference spurs. The non-uniform sampling is due to the fact that the PFD generates variable length pulses aligned to the first occurring edge of the reference clock signal  $f_{ref}$  and the divider signal  $f_{div}$  (Fig. 1): consequently the PFD output is not synchronized to the reference clock. Non-uniform sampling is a highly non linear phenomenon: the contribution of the down-folded noise to the overall output phase noise can be relevant, especially since high frequency and high power  $\Sigma\Delta$  quantization noise is present. Another way of looking at it: it is completely equivalent to non-uniform quantization steps in voltage  $\Sigma\Delta$  DACs.

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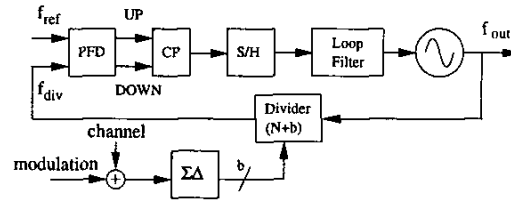


Figure 1: S/H  $\Sigma\Delta$  fractional-N synthesizer

The second advantage of the S/H is its action on the LF voltage. After every UP/DOWN pulse, the S/H samples the voltage across the integrating capacitance and holds it for a reference cycle. This operation prevents the modulation of the LF voltage by the reference clock, hence ideally it eliminates reference spurs [6] in the VCO output. In reality low level spurs may appear at the output due to the charge feedthrough in the control switch. In the next section we derive a linear model for the analysis of the S/H PLL.

## 3. LINEAR MODEL

We first focus our attention on the S/H portion of the PLL. A possible implementation is shown in Fig. 2. This circuit uses a switched-capacitor integrator to carry out both the S/H function as well as the integrator function that is usually implemented by the Loop Filter. To derive the transfer function we start by considering the charge deposited on the capacitance  $C_1$ :

$$Q_{C_1} = \frac{\Delta\varphi(t)}{2\pi} T_{Ref} \cdot I_{CP} \quad (1)$$

where  $\Delta\varphi(t)$  is the phase error waveform produced by the PFD. After a certain delay  $\tau_{SH}$  the charge is transferred to  $C_2$  and added to the charge previously stored:

$$Q_{C_2}(t) = Q_{C_2}(t - T_{Ref}) + Q_{C_1}(t - \tau_{SH}) \quad (2)$$

In voltage terms and inserting the expression for  $Q_{C_1}$ :

$$V_{C_2}(t) = V_{C_2}(t - T_{Ref}) + \frac{I_{CP}}{2\pi \cdot C_2} \cdot T_{Ref} \cdot \Delta\varphi(t - \tau_{SH}) \quad (3)$$

Taking the Laplace transform yields:

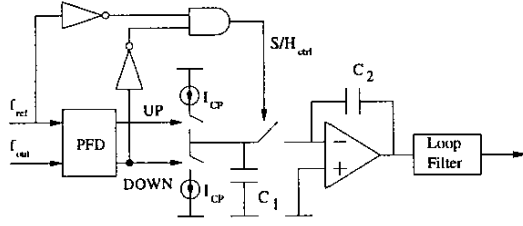


Figure 2: Possible implementation of S/H portion

$$\frac{V_{C2}(s)}{\Delta\varphi(s)} = T_{ref} \cdot \frac{I_{CP}}{2\pi \cdot C_2} \cdot \frac{e^{-s\tau_{SH}}}{1 - e^{-sT_{ref}}} \quad (4)$$

In the previous equation  $V_{C2}(s)$  is still modeled in the discrete-time domain, i.e. as a train of delta-functions. In reality the output voltage is a staircase function. As a consequence eq. 4 is further modified by a zero-order hold network that converts the impulse-train into the staircase waveform. The transfer function of the Zero-order hold network is given by  $H_{ZOH}(s) = \frac{1 - e^{-sT_{ref}}}{s}$ . The actual transfer function from phase difference (PFD input) to integrator output is then given by:

$$\frac{V_O(s)}{\Delta\varphi(s)} = H_{ZOH}(s) \cdot \frac{V_{C2}(s)}{\Delta\varphi(s)} = e^{-s\tau_{SH}} \cdot \frac{I_{CP}}{2\pi \cdot s \cdot C_2} \quad (5)$$

Consequently, the circuit in Fig. 2 can be modeled as shown in Fig. 3. Note that in Fig. 3 the integration  $1/sC_2$  has been absorbed in the loop filter transfer function  $F(s)$ . Thus the only difference introduced by the S/H is the delay  $\tau_{SH}$ . Note that the sampling now always occurs at regular time intervals, namely at the negative edge of the reference clock. In the setup shown in Fig. 2 the delay  $\tau_{SH}$  is equal to half a reference period. The delay is necessary to allow the CP current to be completely integrated before the sampling operation takes place. Note also that the sampling switch needs to be opened while the charge pump is active. The control logic of Fig. 2 takes into account the fact that the rising edge of the DOWN pulse occurs before the rising edge of the reference clock. This results in a variable duty cycle for the  $S/H_{ctrl}$  control signal as shown in Fig. 4.

If a trickle current is used in the CP (e.g. only UP pulses are present) then it is sufficient to invert the reference clock signal to generate a proper  $S/H_{ctrl}$  signal.

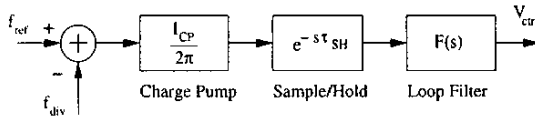


Figure 3: Linear model of S/H portion

### 3.1. Divider

We will now derive a simple linear model for the divider. The first step is to find the timing errors with the aid of Fig. 4.  $N$  is the nominal divider modulus and  $b(n)$  is the dithering value provided by the  $\Sigma\Delta$  modulator. According to the timing diagram we can write:

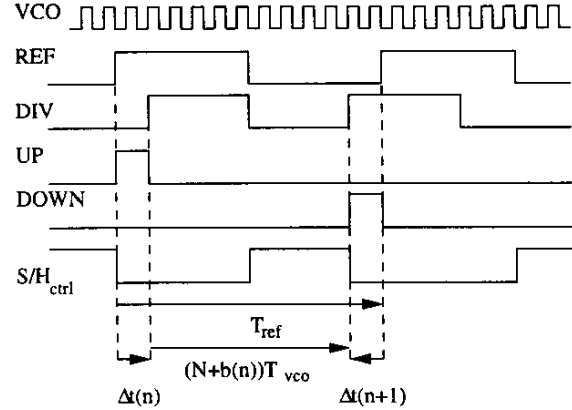


Figure 4: PLL waveforms

$$\Delta t(n+1) = \Delta t(n) + (N + b(n)) \cdot T_{VCO} - T_{ref} \quad (6)$$

Indicating with  $\mu_b$  the average value of  $b(n)$  ( $\mu_b$  is the fractional divider value), the reference period  $T_{ref}$  can be expressed as:

$$T_{ref} = (N + \mu_b)T_{VCO} \quad (7)$$

In deriving eq. 7 we are making the important approximation that  $T_{VCO}$  is constant. This assumption is reasonable for receive-transmit synthesizers with narrow modulation bandwidth. In these cases the relative frequency variation of the VCO is very small, which means that  $T_{VCO}$  is nearly constant.

Defining  $b'(n) = b(n) - \mu_b$  and substituting  $T_{VCO}$  from eq. 7 into eq. 6 yields:

$$\Delta t(n+1) = \Delta t(n) + \frac{T_{ref}}{N + \mu_b} b'(n) \quad (8)$$

Converting to phase domain we have  $\Delta\varphi_{\Sigma\Delta} = \frac{2\pi\Delta t}{T_{ref}}$ . We can finally derive an expression for the additive noise caused by dithering the divider ratio:

$$\Delta\varphi_{\Sigma\Delta}(n+1) = \Delta\varphi_{\Sigma\Delta}(n) + \frac{2\pi}{N + \mu_b} b'(n) \quad (9)$$

The Z-transform yields:

$$\Delta\varphi_{\Sigma\Delta}(z) = \frac{2\pi}{N + \mu_b} \cdot \frac{z^{-1}}{1 - z^{-1}} b'(z) \quad (10)$$

The previous equation shows that the  $\Sigma\Delta$  noise undergoes an integration but is otherwise shaped by the loop in exactly the same way as the reference clock phase noise.

The final linear model is shown in Fig. 5. The closed-loop transfer function  $H_\theta(s)$  is given by (fig: 5):

$$H_\theta(s) = \frac{\frac{I_{CP}}{2\pi} e^{-s\tau_{SH}} \cdot F(s) \frac{K_{VCO}}{s}}{1 + \frac{I_{CP}}{2\pi} e^{-s\tau_{SH}} \cdot F(s) \frac{K_{VCO}}{s} \frac{1}{N + \mu_b}} \quad (11)$$

The phase noise properties can be predicted from linear systems analysis; the  $\Sigma\Delta$  modulation can be modeled as additive phase contribution (also shown in Fig. 5). The  $\Sigma\Delta$  architecture used was a 4<sup>th</sup> order MASH with a 4 bit output signal. The 4 bit quantization causes quantization noise  $n_b$  which is added to the output word. Such noise is spread out over a bandwidth of  $f_{ref} = 1/T_{ref}$

and is high-pass shaped by the  $\Sigma\Delta$  modulator with a noise transfer function (NTF) given by  $H_{NTF}(f) = (1 - e^{-j2\pi f T_{ref}})^4$ . The  $\Sigma\Delta$  signal transfer function (STF) is given by  $H_{STF}(f) = (e^{-j2\pi f T_{ref}})^4$ . Assuming that the quantization noise is independent of the input signal, the power spectral density of the bit stream can be expressed as:

$$S_{nb}(f) = \frac{T_{ref}}{12} |H_{NTF}(f)|^2 \quad (12)$$

From the linear model of Fig. 5 we can find the transfer function from the output of the NTF to the output phase  $\varphi_{VCO}$ :

$$H_n(s) = \frac{2\pi}{N + \mu_b} \cdot \frac{e^{-sT_{ref}}}{1 - e^{-sT_{ref}}} H_\theta(s) \quad (13)$$

Finally the output phase noise Power Spectral Density due to the  $\Sigma\Delta$  quantization noise  $n_b$  is simply given by:

$$S_{\varphi VCO}(f) = |H_n(j2\pi f T)|^2 S_{nb}(f) \quad (14)$$

The effect of quantization error at  $\Sigma\Delta$  input can be evaluated in the same way. The PSD is given by:

$$S_{\Sigma\Delta in}(f) = \frac{T_{ref}}{12} \cdot 2^{-2b_{res}} \cdot |H_{STF}(f)|^2 \quad (15)$$

where  $b_{res}$  is the number of bits below decimal point in  $\Sigma\Delta$  input. The calculation of the power spectral density of the PLL phase error due to the  $\Sigma\Delta$  input quantization is then straightforward (fig. 5):

$$S_{\varphi, \Sigma\Delta in}(f) = |H_n(j2\pi f T)|^2 S_{\Sigma\Delta in}(f) \quad (16)$$

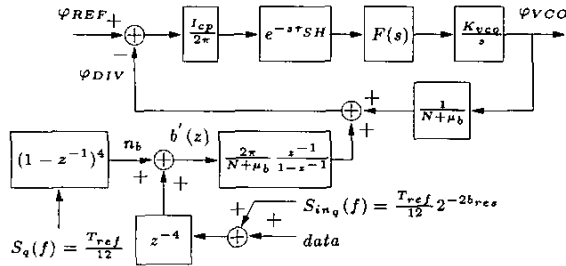


Figure 5: Complete linearized S/H  $\Sigma\Delta$  fractional-N PLL

#### 4. FULLY EVENT DRIVEN SIMULATION

The presence of a multi-bit  $\Sigma\Delta$  modulator makes the use of an event-driven simulator beneficial. Methods based on uniform or adaptive time steps quantize the location of the edges of the sampling time in the  $\Sigma\Delta$  multi-bit quantizer [3]. This is equivalent to non-uniform sampling and leads to down-folding of high frequency noise. The effect is the same as having non uniform steps in multilevel D/A converters.

Besides providing 100% accurate time steps, event driven simulations are very fast and highly efficient: PLL variables are calculated only when an event occurs. The simulation presented in this section is based on a standard event-driven simulator, Verilog XL, customized through PLI (Programming Language Interface) to support mathematical functions.

The simulation set-up is structured in a modularized way: PLL blocks are connected through signals that are responsible for timing and for data exchange. This means that each PLL block can be

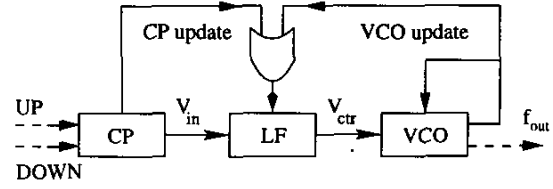


Figure 6: PLL model with Sample/Hold

coded as an independent unit, without worrying about the interaction with the other blocks. The implementation of the synthesizer digital blocks is trivial; we concentrate on the implementation of the Loop Filter which is the biggest issue in PLL simulations.

The following discussion is focused on the LF modeling, but it applies to any (pseudo) continuous time system modeling. The way the Loop Filter is modeled is shown in Fig. 6. Every time a control signal is issued from the VCO or the CP, the loop filter updates its state and calculates a new control voltage according to the actual input value.

To describe the LF behavior in mathematical terms we start from its transfer function and we derive its State-Space Formulation. We assume the LF transfer function to be given by the following equation:

$$F(s) = \frac{1 + \frac{s}{s_0}}{sC \cdot \left(1 + \frac{s}{p_0}\right) \cdot \left(1 + \frac{s}{p_1}\right) \cdot \left(1 + \frac{s}{p_2}\right)} \quad (17)$$

Note that equation 17 also includes the integrating capacitance. With a partial fraction expansion, equation 17 can be decomposed into 4 parallel blocks, namely an integrator and three 1<sup>st</sup> order RC blocks. Noting that between the update times the input to the LF is constant (e.g.  $V_{in}$  is appearing as a staircase to the LF), the equation describing the behavior of each of the three RC blocks is given by (state equation solution):

$$V_x(t_1) = V_x(t_0) + (A_x V_{in}(t_0) - V_x(t_0)) \left(1 - e^{-\frac{t_1 - t_0}{\tau_x}}\right) \quad (18)$$

The equation that describes the integrating block is given by:

$$V_C(t_1) = V_C(t_0) + \frac{A_0 V_{in}(t_0)}{C} (t_1 - t_0) \quad (19)$$

The VCO control voltage is then given by:

$$V_{ctr}(t) = V_1(t) + V_2(t) + V_3(t) + V_C(t) \quad (20)$$

The Verilog model for the LF is then simply given by a set of equations which describe exactly the behavior of the LF. The VCO is modeled as a self-updating block. Such operation can be visualized as shown in Fig. 6. The update takes place at discrete time instances, namely every half-VCO period. The approximation introduced is minimal, since the frequency of the VCO is several orders of magnitude higher with respect to the PLL dynamics. Every half-period the VCO sends an update signal to the LF to obtain the new VCO control voltage; on the basis of the updated value, the new VCO period is calculated. Note that the LF update takes place only when required by other blocks: the update time intervals are not uniform. This makes the simulation methodology very efficient, since the calculations occur only at the required time steps.

## 5. RESULTS

The methodology described in section 4 was used to simulate the topology presented in section 2. Fig. 7 shows the Power Spectral Density (PSD) of the output phase noise  $\varphi_{VCO}$  due to the  $\Sigma\Delta$  quantization for two different cases. The lower curves represent the ideal condition: the input data to the  $\Sigma\Delta$  presents no input quantization. The upper curves are instead the result of a 16 bits quantization below decimal point. The curves obtained from the simulation (PSD calculated with Matlab) match perfectly the PSD described by equations 14 and 16.

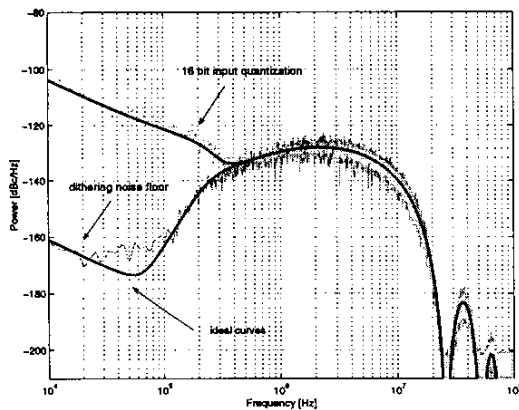


Figure 7: Synthesizer Phase Noise PSD

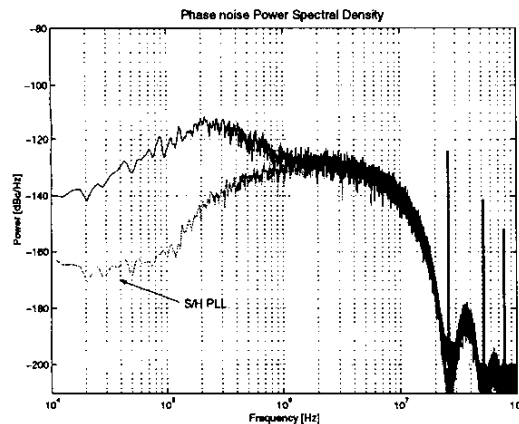


Figure 8: Phase Noise PSD: S/H PLL vs. regular PLL

The low frequency noise floor is due to a very small amount of dithering applied on the  $\Sigma\Delta$  modulator input. In absence of modulated data, dithering is necessary to avoid the presence of fractional spurs. Note that no reference spurs appear in the output spectrum.

In figure 8 the PSD of the S/H PLL is compared with the PSD of the standard PLL. The S/H PLL has a lower overall phase noise and does not present reference spurs which appear instead in the spectrum of the standard PLL (i.e. without S/H).

As already discussed in section 2, reference spurs may appear also in the S/H PLL output when a real switch is used to control the

S/H. However the level of such spurs would be much lower with respect to the spurs level of a standard PLL. Besides, the spurs level for a standard PLL is higher in real situations, when CP mismatches, CP leakage currents and timing mismatches in the PFD are taken into account. Even in ideal conditions, the spurs are exceeding the GSM mask specifications. Simulations have shown that the S/H PLL does not present spurs even in case of CP mismatches and CP leakage currents.

Real GSM data was fed into the  $\Sigma\Delta$  modulator through a digital prewarp filter. The output spectrum lies within the mask specified by the GSM standard and the RMS phase error is smaller than 0.5 deg RMS. This indicates that the S/H PLL is suitable for direct GSM modulation.

## 6. CONCLUSIONS

This work presented a new  $\Sigma\Delta$  fractional-N synthesizer topology and a new simplified theory to describe the PLL performance. Also, a new simulation methodology completely based on event driven approach is shown. The novelty is represented by the introduction of a S/H block to avoid noise down-fold due to the non-uniform sampling operation of the PFD. The S/H also eliminates the problem of reference spurs in the VCO output. We have shown how it is possible to represent the behavior of the loop filter in a way which is suitable for event-driven based simulations. Extremely high accuracy can be reached because undesirable time quantization phenomena are avoided, the only limit being the numerical accuracy of the event-driven simulator. The simulations are very fast since they proceed through events and the implementation is straightforward. The comparisons presented in section 5 demonstrate the advantages of the S/H PLL over a standard PLL and they show the perfect match between the theoretical model and the simulations. Finally, the S/H PLL fulfills the GSM standard both in receiving and transmitting mode.

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